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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,861	05/24/2000	Timothy J. Williams	0325.00339	4837

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EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	10

DATE MAILED: 06/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/577,861	WILLIAMS, TIMOTHY J.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 2, 2004 has been entered.

2. Claims 1-25, as per Amendment C filed March 3, 2004, are pending.

3. Claims 1 and 15 are objected to because of the following informalities: "predetermine delay" is interpreted as –predetermined delay–. Appropriate correction is required.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-3, 5-12, 15, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aab, U.S. Patent No. 6,357,012, in view of Philips Semiconductors, "74HC/HCT5555 Programmable delay timer with oscillator", September 1993 ("Philips").

As per claim 1, Aab teaches an apparatus comprising:

a timer circuit configured to present a wake-up signal in response to an input signal (Fig. 1, time-switch logic 16 presents wake-up signal on line 26 in response to signal on line 25); and

a microcontroller configured (i) to exit a suspend or sleep mode in response to said wake-up signal (Col. 3, lines 1-21, in response to line 26, microcontroller core 11 is brought out of inactive state) and (ii) to generate said input signal, wherein said input signal comprises a programmable delay value determined by said microcontroller during an awake mode in response to said wake-up signal (Col. 3, lines 1-21, "a specific elapsed time span, which is

determined during the active phase of the microcontroller core 11, and is set via line 25") and a predetermined delay value (Col. 4, lines 44-56, "transient recovery time").

However, Aab does not expressly teach details of the timer circuit such as presenting any of a plurality of divided delay signals as a wake-up signal. Phillips teaches a timer circuit configured to present any of a plurality of divided delay signals (Figs. 3 & 4, 24-stage counter; Page 2, divide-by range of 2 to 2^{24}) in response to programmable delay value and an enable signal (Page 2, pinning; Fig. 3, programmable inputs S_0 to S_3 and trigger input A or B). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the details of Philips' timer circuit to Aab's apparatus. A motivation for doing so would have been to ensure the integrity of the timer circuit. Furthermore, since Philips timer circuit requires an enable signal to trigger a wake-up signal, it would have been obvious to have Aab's apparatus present such an enable signal to the timer circuit.

As per claims 2 and 3, Philips teaches a timer input signal comprising a programmable multi-bit signal (Fig. 3, inputs S_0 to S_3).

As per claim 5, Aab teaches a wake-up delay timing value (Col. 3, lines 1-21).

As per claim 6, Philips teaches said timer circuit comprises:

a delay circuit configured to generate a delay signal (Page 4, first paragraph); and

a select circuit configured to (i) generate said plurality of divided delay signals and (ii) and present said wake-up signal in response to said delay signal and said input signal (Fig. 4).

As per claim 7, Philips teaches said input signal is configured to control selection of one of said plurality of divided delay signals for presentation as said wake-up signal (Fig. 4).

As per claim 8, Philips teaches each of said divided delay signals has a period that comprises a multiple of a period of said delay signal (Page 2, divide-by range of 2 to 2^{24}; Page 4, "counter divides the frequency to obtain a long pulse duration").

As per claim 9, Philips teaches said select circuit is configured to multiplex said plurality of divided delay signals in response to said input signal (Fig. 4).

As per claim 10, Philips teaches said select circuit comprises:

a divider circuit configured to generate said plurality of divided delay signals in response to said delay signal (Fig. 4); and

a multiplexer configured to present said wake-up signal in response to said plurality of divided delay signals and said input signal (Fig. 4).

As per claim 11, Philips teaches said timer circuit comprises a counter configured to generate each of said plurality of divided delay signals in response to a different value of said input signal (Fig. 4).

As per claim 12, Philips teaches said delay circuit is further configured to present said delay signal in response to an enable signal (Fig. 3, trigger inputs A or B).

As per claims 15, 16, 18 and 19, since Aab/Philips teaches the apparatus of claims 1-3 and 5-12, the combination teaches the claimed method.

6. Claims 4, 13, 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aab/Philips as applied to claim 1 above, and further in view of Borras, U.S. Patent No. 5,128,938.

As per claim 4, Aab/Philips does not expressly teach the microcontroller operating in response to firmware instructions. Borras teaches determining a programmable delay value in response to one or more firmware instructions (Col. 4, line 66 – Col. 5, line 10). At the time of the invention it would have been obvious to one skilled in the art to apply Borras' firmware instructions to Aab/Philips' microcontroller. A motivation for doing so would have been to ensure the integrity of microcontroller operation.

As per claim 13, Borras teaches said input signal is generated in response to a value stored in a register of said second circuit (Col. 4, line 66 – Col. 5, line 10).

As per claim 17, since Aab/Philips/Borras' teaches the apparatus of claim 4, the combination teaches the claimed method.

As per claim 22, Borras teaches said first circuit is configured to periodically wake up said second circuit and a sleep period of said second circuit is determined by said programmable delay value (Fig. 3).

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aab/Philips as applied to claim 1 above, and further in view of Horowitz & Hill, The Art of Electronics, Cambridge University Press, Second Edition, Chapter 10, pp. 673-674, 1999.

As per claim 21, Aab/Philips is silent with regards to implementing said timer circuit and said microcontroller on a single integrated circuit. Horowitz & Hill teaches that it common to implement a microcontroller as an integrated circuit with on-chip components for optimization purposes (paragraph continued from page 673 to page 674). Thus it would have been obvious to

one of ordinary skill in the art to implement Aab/Philips timer circuit and microcontroller as a single integrated circuit.

8. Claims 14 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aab, U.S. Patent No. 6,357,012, in view of Philips Semiconductors, "74HC/HCT5555 Programmable delay timer with oscillator", September 1993 ("Philips") and Horowitz & Hill, The Art of Electronics, Cambridge University Press, Second Edition, Chapter 10, pp. 673-674, 1999.

As per claim 14, Aab teaches a microcontroller circuit comprising:

a controller (Fig. 1, microcontroller core 11) configured (i) to operate in a sleep mode and a wake-up mode (Col. 3, lines 1-21, inactive and active operating states) and (ii) to generate an adjust signal (Col. 3, lines 1-21, "via line 25"), wherein said adjust signal is determined in response to a wake-up signal (Col. 3, lines 1-21, in response to signal on line 26) and a predetermined delay value (Col. 4, lines 44-56, "transient recovery time") during said wake-up mode; and

a timer circuit configured to control switching of said controller from said sleep mode to said wake-up mode after a programmable period of time (Fig. 1, timer-switch logic 16; Col. 3, lines 1-21, "a specified elapsed time span").

However, Aab does not expressly teach details of the timer circuit. Philips teaches a timer circuit that comprises:

(i) a delay block configured to generate a delay signal in response to an enable signal (Fig. 3, oscillator configuration generates delay in response to trigger inputs A or B) and

(ii) a divider circuit configured to generate a plurality of divided delay signals in response to said delay signal (Fig. 3, 24-stage counter), where said plurality of divided delay signals determine a range of said programmable period of time (Page 2, divide-by range of 2 to 2^{24}) and said timer circuit is configured to select one of said plurality of delay signals as said wake-up signal in response to an adjust signal (Fig. 4, in response to programmable inputs S_0 to S_3).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the details of Philips' timer circuit to Aab's microcontroller circuit. A motivation for doing so would have been to ensure the integrity of the timer circuit. Furthermore, since Philips timer circuit requires an enable signal to trigger a wake-up signal, it would have been obvious to have Aab's microcontroller circuit present such an enable signal to the timer circuit.

While Aab teaches integrating components into the microcontroller circuit (Col. 1, lines 35-45), Aab does not expressly teach the microcontroller circuit as an integrated circuit. Horowitz & Hill teaches that it common to implement a microcontroller as an integrated circuit with on-chip components for optimization purposes (paragraph continued from page 673 to page 674). Thus it would have been obvious to one of ordinary skill in the art to implement Aab/Philips' microcontroller circuit as an integrated circuit.

As per claim 25, Aab teaches said controller is configured to determine a value for said adjust signal that produces said programmable period of time (Col. 3, lines 1-21).

9. Claims 20, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aab/Philips as applied to claims 1 and 15 above, and further in view of Lee et al., U.S. Patent No. 6,025,745 ("Lee").

As per claims 20, 23 and 24, Aab/Philips does not expressly teach calibrating a programmable delay circuit. Lee teaches the steps for calibrating a delay circuit (Fig. 3). At the time of the invention, it would have been obvious to one of ordinary skill in the art to Lee's calibrating to Borras/Philips' method in order to adjust delay to account for variations such as those due to variations in environment and manufacture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
June 11, 2004

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